Design of the Advanced Light Source Timing System*

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Abstract
The Advanced Light Source (ALS)[1] is a third generation synchrotron radiation facility, and as such, has several unique timing requirements. Arbitrary Storage Ring filling patterns and high single bunch purity requirements demand a highly stable, low jitter timing system with the flexibility to reconfigure on a pulse-to-pulse basis. This modular system utilizes a highly linear Gauss Clock with "on the fly" programmable setpoints to track a free-running Booster ramping magnet and provides digitally programmable sequencing and delay for Electron Gun, Linac, Booster Ring, and Storage Ring RF, Pulsed Magnet, and Instrumentation systems. It has proven itself over the last year of accelerator operation to be reliable and rock solid.

I. INTRODUCTION

ALS consists of an Electron Gun with a gated 125 MHz repetition rate. The gun injects into a 3 GHz 50 MeV Linac providing acceleration to the injection energy of the 500 MHz Booster Synchrotron. A Peaking Strip and Gauss Clock track the slope of the Booster Bend Magnet ramp, providing field-derived triggers for the various injection systems.

The 1 Hz Injection/Booster system allows up to twelve 500 MHz buckets to be bunched, accelerated and stored each cycle. When extracting beam from the Booster, an array of fast pulsed magnets are individually triggered by programmable digital timers, referenced to the Gauss Clock, so that their extraction fields coincide with the arrival of beam.

The timing system features a very flexible Storage Ring loading scheme that targets accelerated bunches into Storage Ring buckets as defined by a spreadsheet-based control program. The targeted buckets can be re-targeted on a cycle-to -cycle basis, and can be loaded into any combination of Storage Ring buckets and in any order.

II. HARDWARE

We use Eurocard 3U modules for most of our low level construction. We found no difficulty passing high speed logic signals across the 96-pin DIN connector using adjacent pins and differential format. One double rack was reserved for timing system components, of which 40% is available for future development.

Test points are brought to SMA connectors on the front panel and are individually buffered. ECL signals leaving a module are always differential and routed in twisted pairs.

To control temperature rise, each module was limited to four watts dissipation. No blowers are used, so cooling is entirely by conduction & convection.

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III. LOGIC FAMILY SELECTION

An early problem was the choice of a logic family. The timing system frequently uses 500 MHz clock frequencies, and even when lower frequencies are used, preservation of edge resolution is crucial. Conventional TTL logic is totally incapable of performing in this area; even conventional ECL logic is pushed beyond its capabilities. Gallium Arsenide logic was available, but costs were quite high. A variant of ECL called ECLiPS (ECL in PicoSeconds)[2] was introduced by Motorola that fit our needs. ECLiPS handles speeds almost three times as high as conventional ECL and dissipates half the power. It uses conventional ECL logic levels and is packaged in a 28-pin PLCC surface mount package.

IV. PC BOARD DESIGN

Due to the very high edge speeds (300 ps) of ECLiPS, the printed circuit layout must follow guidelines similar to UHF RF designs[3]. All signal lines are configured as 50 Ohm strip lines or microstrip lines and are terminated at their destinations. Low impedance ground planes and power planes help maintain good noise margins. A four-layer board with onesignal plane was adopted for simple designs and a six-layer board with two signal planes is used for more complex layouts.

FR-4, a glass epoxy based substrate, was chosen for economy. The dielectric constant is not tightly controlled, but is quite adequate for this service. True "RF grade" substrates tend to have high dielectric constants, which increase the propagation delays, and are significantly more costly.

V. CONTROL SYSTEM

The control system in use at the Advanced Light Source is based on a custom-designed controller, the ILC (Intelligent Local Controller) [4, 5]. An ILC is installed in each timing system bin that requires real-time external control. Timing system modules are designed with addressable registers so that they can be programmed from an ILC 8 bit I/O port. Addressing is done via a second 8 bit port and up to 16 four byte registers can be serviced by a single ILC.

VI. TIMING SCHEME

Timing for the ALS is based on three epochs. These separate epochs are necessary because the Booster Bend Magnet is driven by an unregulated voltage. Current (and field) will rise at the L/R time constant (0.71 sec.) of the magnet.

Epoch 1 is driven by a line sync'd clock at the Booster rep-rate, nominally 1 Hz. Its function is little more than "Phasing On" the Booster Bend Magnet power supply, and some long lead-time, low criticality systems.

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Epoch 2 is defined by the Bend Magnet reaching the field strength necessary to bend the injected 50 MeV electrons around the Booster Ring. This point is determined by measurement of the magnetic field with the Gauss Clock system. Epoch 2 is the basis of timing for the Electron Gun, Linac, and Booster Injection Kicker.

Epoch 3 is defined by the Bend Magnet reaching the field strength consistent with the desired final booster energy, nominally 1.24 Tesla @ 1.5 GeV. The Gauss Clock system, again, provides the signal. Epoch 3 is the basis of timing for extraction from the Booster and injection into the Storage Ring, including kickers, septum, and bump magnets. The Booster Bend Magnet ramp is terminated several milliseconds after Epoch 3.

VII. CLOCKS

There are 4 clocks utilized in the timing system, all but one (line sync) are derived from the 500 MHz (499.654 MHz to be precise) RF Master Oscillator:

60 Hz - Derived from power line, used to establish basic repetition rate of the machine.

Booster Ring Orbit Clock (BROC) - 4 MHz (500 MHz/125), 250 ns. This is the period of one revolution of an electron in the Booster Ring.

Storage Ring Orbit Clock (SROC) - 1.523 MHz (500 MHz/328), 657 ns. This is the period of one revolution of an electron in the Storage Ring.

Coincidence Clock (COIC) - 12.19 KHz (500 MHz/(125*328)), 82 us. Marks the beginning of the pseudorandom intersection pattern of the Booster and Storage Ring Buckets. More on this later.

VIII. GAUSS CLOCK SYSTEM

Booster Ring injection and extraction timing are primarily dependent upon the field in the Booster Bend Magnet. The magnet power supply is turned on at the beginning of each Booster cycle (Epoch #1) and the current is allowed to ramp up on the magnets' L/R time constant. It is not possible to predict, with the required accuracy, just when the field will be proper, because the power supply voltage is unregulated and residual magnetism is left in the magnet core. The Gauss Clock system provides real-time magnetic field tracking and a set of programmable trip points, which can be set in absolute Gauss via an ILC.

The timing system is composed of:

Peaking Strip—A RF-excited sensing coil array[6] wound on a Permalloy strip is used to detect when the Bend Magnet field reaches 100 Gauss.

Pickup Coil —A one-turn shielded loop wound around the pole of one of the 24 series-connected Bend magnets. The voltage induced into the loop is directly proportional to the rate of rise of the magnets field.

Voltage to Frequency Converter—An amplifier and highly linear Quartz controlled V/F converter convert the loop voltage to a logic compatible pulse rate in the 1 to 2 MHz range.

Programmable Counter Modules—24 bit programmable downcounters that, when preset by the ILC, will output a pulse when the downcount reaches zero.

At magnet turn-on time, there exists some unknown residual field in the magnet core; this field adds to the field induced by the now-ramping magnet current. When this sum is sufficient to counteract a bias field set up in the peaking strip, an inversion of the magnetization in the Permalloy strip occurs. A short output signal results. The bias field is set so that this inversion occurs at about 100 gauss.

When the Peaking Strip signals that the Bend Magnet field has crossed 100 Gauss, the Counter modules begin counting the output of the V/F converter. The counters are, in fact, integrating the rate of rise, and the count, at any instant, is proportional to the absolute field (less the 100 Gauss starting point). A bank of these counters, each preset to look for its dedicated field intensity, count in parallel, providing triggers for injection, extraction, Booster Bump magnet triggering, and instrumentation. One counter provides a burst of 100 equi-gauss spaced sampling pulses used to control tracking of focusing and corrector magnets with the Booster Bend magnet.

IX. INJECTION LINE TIMING

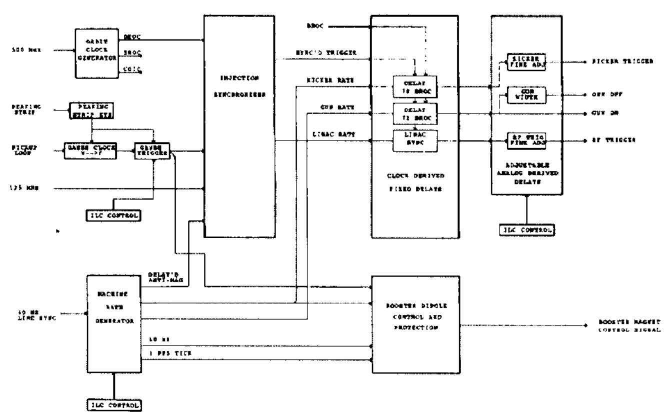
The Injection system must produce gated bursts of electron bunches at a 125 MHz rate. The bursts may contain one to twelve bunches, and will nominally occur at one burst per second. The bunch width is nominally two nanoseconds.

Burst gate timing is dependent on:

1. Desired repetition rate.
2. Booster Bend Magnet attaining injection field.
3. Phase of Booster Ring Orbit Clock (BROC).
4. Phase of 125 MHz RF signal.

The last two dependencies exist so that an electron burst, when steered into the Booster, will always begin in bucket #1 (thus greatly simplifying the task of timing for transfer into a selected bucket in the Storage Ring). When all four conditions are met, a synchronized trigger results. This is Epoch 2. This trigger will fire the Electron Gun[7], start the RF system, and trigger the Injection Kicker magnet so that the beam arrives just as the Kicker reaches its flattop region. The Buncher and Linac RF system is triggered about 16.5 uS prior to beam arrival at the Buncher. Its timing system[8] generates the individual gates for RF system components.

Booster Injection Timing



Each of these functions must have versions of the Epoch 2 trigger to compensate for pre-trigger requirements and electron time of flight. The gross delays are achieved by digital countdown of the BROC period while fine adjustment delays are done with an Analog Devices AD-9500 very fast analog timer chip.

X. TARGETING THE STORAGE RING

Imagine, for a moment, the Booster and Storage rings as a pair of intersecting mechanical gears. The Booster gear has 125 teeth, corresponding to its 125 beam buckets, and the Storage gear has 328 valleys. Now paint the current intersection of the Booster tooth and Storage valley white, this will mark bucket #1 of each ring.

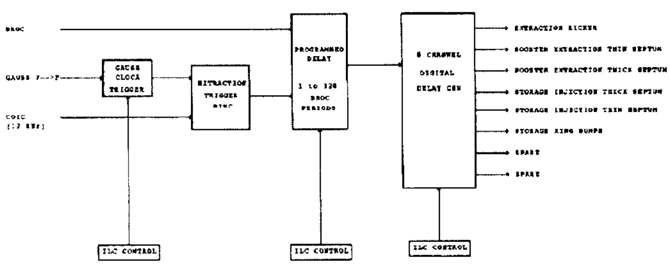
Each time the Booster gear revolves, tooth #1 will intersect a different Storage gear valley, 1, 126, 251, 48, 173, etc., each valley is offset 125 from the last. This series continues unrepeating until Booster tooth #1 has met all 328 Storage gear valleys (328 Booster revolutions). This is the period of the COIC clock.

Discarding the gear analogy, you see that once Booster Ring beam has reached the desired energy, it can be injected into any Storage Ring bucket simply by delaying injection by "n" BROC periods from COIC. "n" is derived from an equation which is a function of the target bucket number (1-328). A programmable up counter is loaded by the ILC with 2's complement of "n."

$$n = (21 \times t) \text{ modulus } 328$$

where "t" is the target bucket in the Storage Ring and "n" is the required number of Booster Ring revolutions after COIC necessary to line up the Booster beam with the target bucket.

ALS Extraction Timing



Storage Ring loading requirements mandate an agile control scheme. Accelerated beam will be placed into Storage Ring orbit at positional offsets (buckets) that may vary from pulse to pulse. An "Intelligent Local Controller" (ILC) is dedicated to controlling this process and is provided with a 1 Hz (Epoch 1) interrupt to insure lockstep with Booster cycles.

A Storage Ring loading pattern table is downloaded to the ILC from an EXCEL spreadsheet application. This table has an entry for each Booster cycle, and may include;

A. Target Bucket number.
B. Beam Dump trigger.
C. Idle Mode command.
D. Flow commands such as START, STOP, PAUSE, REPEAT, etc.

The ILC interrupt steps the table to the next entry and sends appropriate commands to the hardware.

The loading table is prepared off-line and stored on disk; the operator simply chooses a table from the list and tells the Accelerator Control system to load and start it. The table will execute until it encounters a Stop command or is manually terminated.

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XII. REFERENCES

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